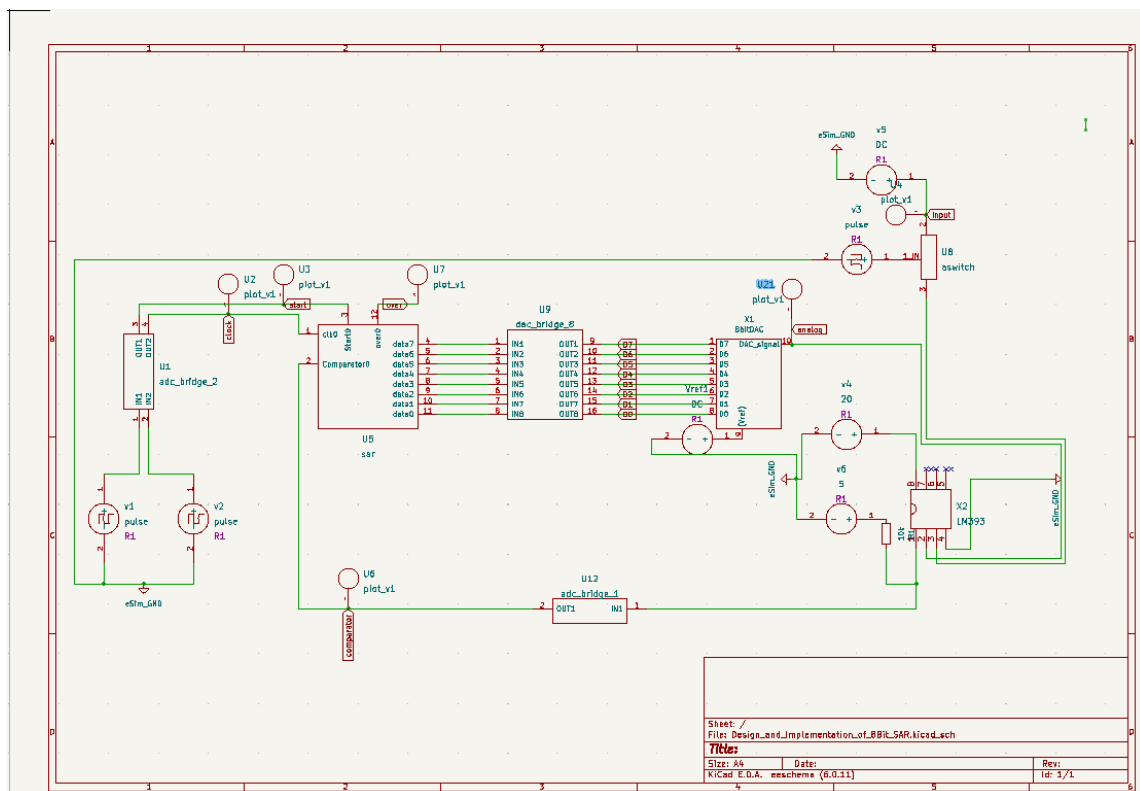


Title of the circuit :Design and Implementation of 8-bit Successive Approximation Register (SAR) ADC

Theory/Description :

A Successive Approximation Register (SAR) ADC is a type of analog-to-digital converter .It operates using a **binary search algorithm** to converge on the digital equivalent of an analog input voltage. The SAR ADC is widely used in data acquisition systems, embedded devices, and mixed-signal circuits because of its medium-to-high resolution (8–16 bits) and relatively fast conversion rates. The basic blocks of an 8-bit SAR ADC are:

1. **Successive Approximation Register (SAR)** – a digital logic block that performs the binary search by successively setting and clearing bits from MSB to LSB.
2. **Digital-to-Analog Converter (DAC)** – generates an analog voltage corresponding to the current SAR output code.
3. **Comparator** – compares the DAC output with the input signal and provides feedback to the SAR logic.
4. **Sample and Hold Circuit** – captures the analog input voltage and holds it constant during conversion.



1) SAR BLOCK :

The **Successive Approximation Register (SAR) block** was designed in **Verilog** to implement the digital control logic of the SAR ADC. The module takes in three primary inputs:

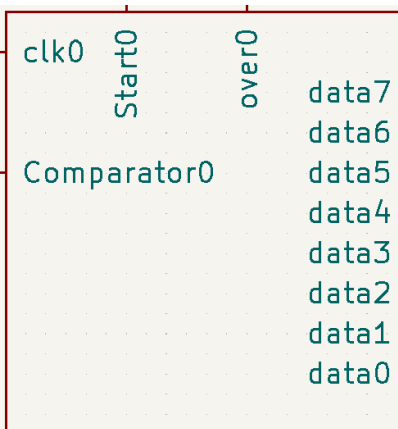
- **clk** – system clock signal that synchronizes the bit trials.
- **Comparator** – indicates whether the DAC output is greater or less than the input analog voltage.
- **Start** – signal to initiate a new conversion cycle.

The module outputs:

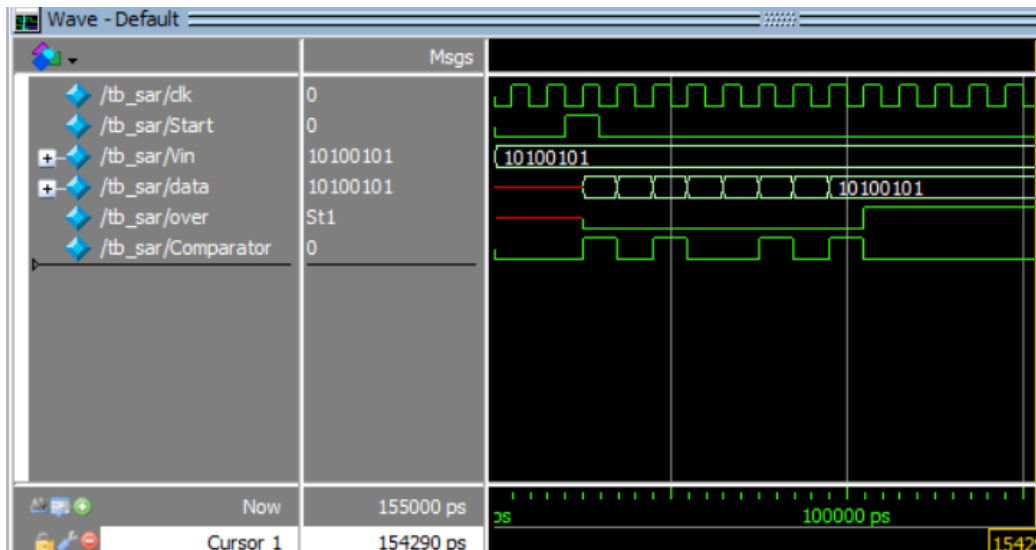
- **data [7:0]** – the final 8-bit digital output corresponding to the analog input voltage.
- **over** – flag signal that goes high once the conversion process is complete.

The correctness of the SAR logic was verified in Quartus using a testbench . Waveforms and output values from the simulation confirmed that the SAR logic functions correctly and generates the expected 8-bit digital codes. The Verilog files used have been added in the Research Migration Directory .

SAR Block creating using NGVeri .

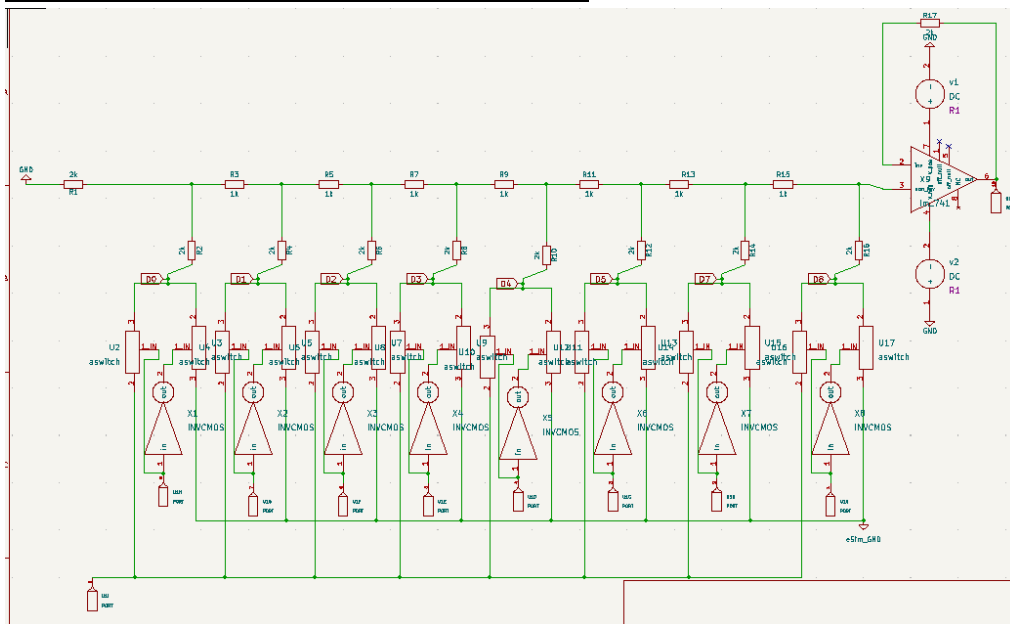


Testbench waveform:



- Gets converted in 8 clock cycles after start signal .

2) DAC (R-2R Network) subcircuit block:



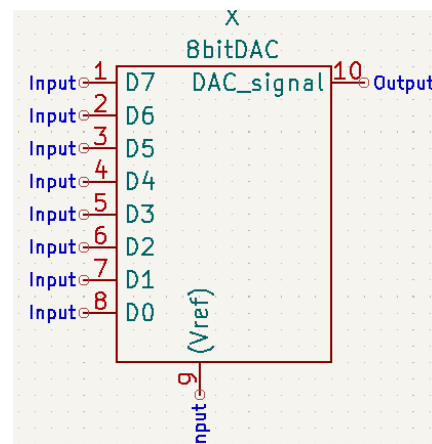
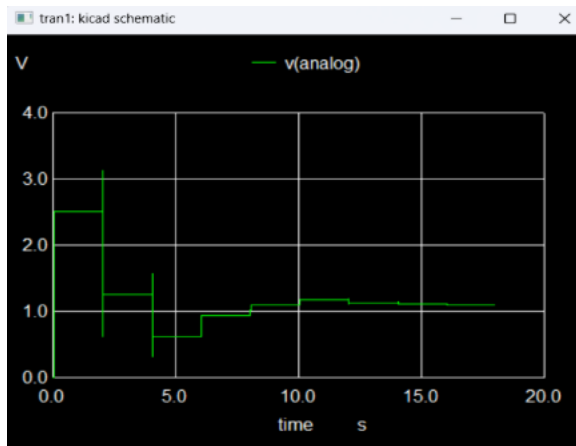
The **R-2R ladder** is a simple and efficient resistor network used to convert a digital code into an analog voltage. It requires only two resistor values: **R** and **2R**. By arranging these resistors in a repetitive ladder structure, each digital input bit contributes a precisely weighted current to the output.

- Each digital input controls a **switch** that connects a node in the ladder either to a reference voltage (**Vref**) if the bit is “1” or to ground if the bit is “0.”

- The resistor network ensures that:
- The **Most Significant Bit (MSB)** contributes half of the full-scale output.
- The next bit contributes one-quarter, the next one-eighth, and so on, down to the **Least Significant Bit (LSB)**.
- These contributions add up linearly at the output node, giving an analog voltage proportional to the digital code.

Formula : $V_{out} = V_{ref} * (\text{Digital Code} / 2^N)$

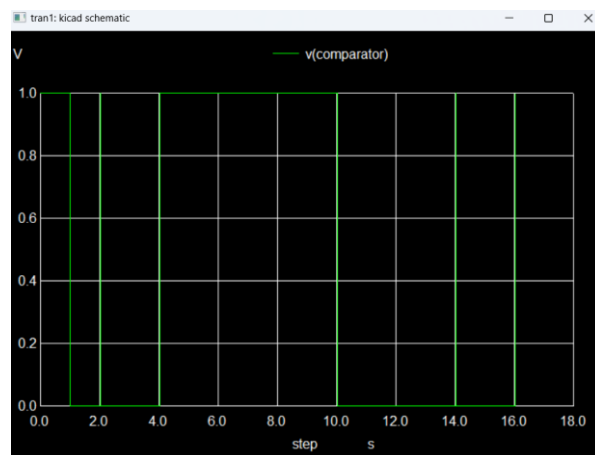
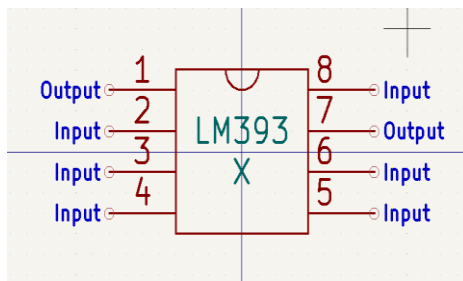
- **Digital code = 1000 0000 = 128 , $V_{out} = 5 * (128/256) = 5 * 0.5 = 2.5$.**



Output with $V_{ref} = 5V$ and $V_{in} = 1V$

DAC block

3) COMPARATOR BLOCK (LM393)



In the given circuit, a **LM393 comparator** is used to compare the analog voltage generated by the **R-2R (DAC)** with the applied input voltage V_{in} .

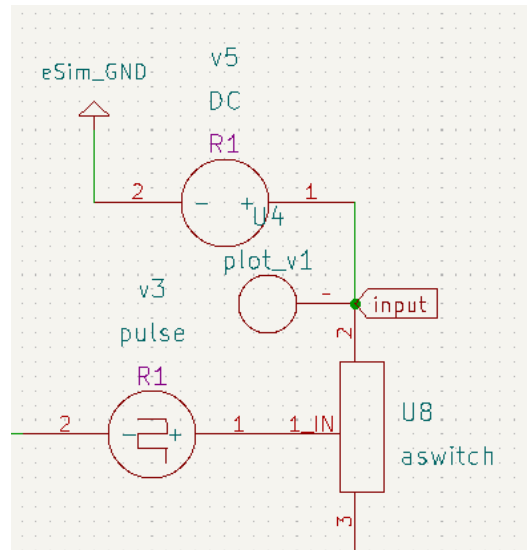
- **Pin 8 (Vcc):** The comparator is powered using a +20 V supply. This ensures the internal transistors operate correctly and allows the comparator to handle higher voltage ranges.
- **Pin 4 (Ground):** Connected to the ground reference of the circuit.
- **Pin 2 (Inverting Input, V_-):** Receives the analog voltage V_{dac} from the R-2R ladder DAC. This voltage corresponds to the digital input code applied to the DAC.
- **Pin 3 (Non-Inverting Input, V_+):** Receives the reference input signal V_{in} . This is the test voltage against which the DAC output is compared.
- **Pin 1 (Output):** The LM393 has an open-collector output, which requires a pull-up resistor to a logic supply 5V in this schematic. The output is thus pulled to 5 V or 0 V, depending on the comparison result.

4) **SAMPLE AND HOLD**

In the initial design, the Sample and Hold (S&H) block was unable to accurately track sine-wave input signals. The main issue was that the S&H could not reliably capture and hold the instantaneous value of the sine wave at the correct sampling instants. In addition, clock mismatches between the SAR logic and the S&H control introduced synchronization errors. Together, these effects led to significant deviations in the voltage presented to the comparator, reducing conversion accuracy for analog signals.

To explore possible improvements, I attempted an alternative approach. Instead of a conventional S&H, an analog switch (aswitch) was used. This switch is triggered after the **Start** signal and is driven by the **same clock** as the SAR controller. The intention was to synchronize the input sampling with the SAR conversion steps, thereby minimizing timing mismatches.

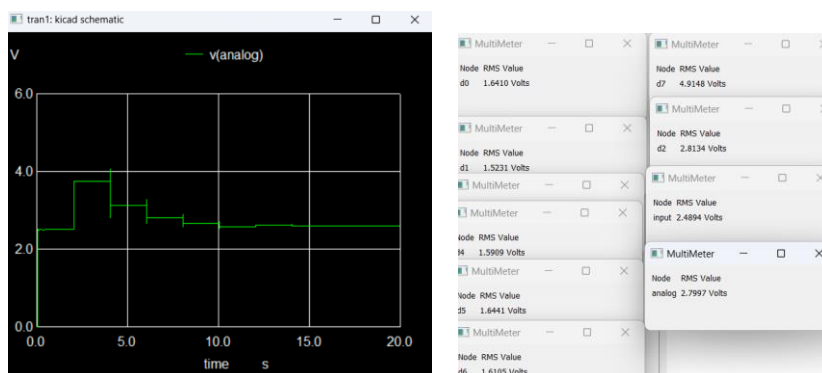
However, this approach did not fully solve the problem. The aswitch-based method worked reasonably well when the input was a **DC source**, since the voltage remained constant during conversion. But for time-varying signals (such as a sine wave), the lack of proper peak tracking meant that the comparator still received inconsistent values. As a result, the overall system continues to be limited to DC inputs.



OUTPUT:

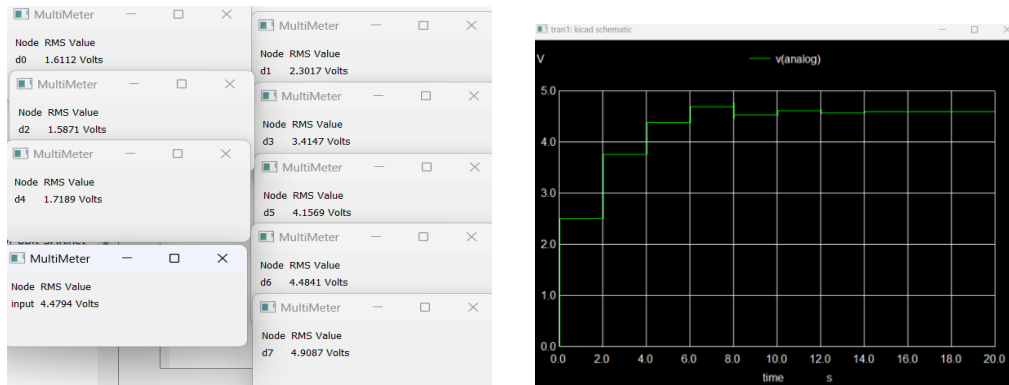
1) $V_{in} = 2.5 \text{ V}$, $V_{ref} = 5 \text{ V}$, Actual code = 1000 0000 , Output Code = 1000 0100 = 132

$$V_{out} = 5 * (132/256) = 2.56$$



2) $V_{in} = 4.5 \text{ V}$, $V_{ref} = 5 \text{ V}$, Actual code = 11100110 , Output Code = 11101010 = 234

$$V_{out} = 5 * (234/256) = 4.57$$



Analysis of Accuracy and Limitations in the Current SAR ADC Design

- The current SAR ADC gives about **98% accuracy**, which is good for basic use but still has limits. The main problem is with the **Sample and Hold (S&H) circuit**, as mentioned before, which can only work properly with **DC inputs**. Because of this, the circuit cannot handle **changing signals like sine waves**, where the voltage must be sampled exactly at the right moment. Without a proper S&H, the comparator does not always get the correct value during conversion.
- Another limitation is the **reference voltage (V_{ref})**. Right now, the circuit can only support a maximum of **12 V**. This is enough for testing, but if the circuit could handle a wider range of reference voltages, it would be more flexible and easier to use with different sensors.

Source/Reference(s) :

1) [Understanding SAR ADCs: Their Architecture and Comparison with Other ADCs | Analog Devices](#)

2) [IJSSPR 8104 3129 https://www.ijsspr.com/citations/v8i1n4/IJSSPR_8104_31293.pdf](https://www.ijsspr.com/citations/v8i1n4/IJSSPR_8104_31293.pdf)

